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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 34

Application Number: 09/261,081
Filing Date: March 02, 1999
Appellant(s): SOOHOO, KENNETH

George A. William
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 29, 2003

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 30-38 and 67, 68 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,208,319	NISHIDA	3-2001
5,555,360	KUMAZAKI et al.	9-1996

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 30-38, 67 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishida in view of Kumazaki et al., U.S. Patent Number 5,555,360.

As per independent claim 30, a system for display a character . . . comprising: receiving a command to generate the shape . . . a particular size on a display, requesting a bit map rendering of the shape . . . larger than the particular size, wherein various portions of the bit map correspond to a pixel; and among the various bits . . . different bits correspond to different locations on the character; based on a percentage of bits that are on . . . determining luminances for the corresponding pixels . . . having the particular size; and displaying the shape . . .

Nishida discloses a display device having a divisional level represented by bit or bits recognizable by the address information for the divisional level, bit map, col. 3, lines 21-30 . . . determines luminance for corresponding pixels; and logic that causes the character to be displayed in the region . . . Nishida discloses state in which the operations turn on the bulb in the predetermined luminance values, col. 19, lines 1-21.

However, it is noted that Nishida fails to disclose a vector representation of the bit map. Kumazaki et al. discloses an antialiasing system for determining the luminance of the edge pixels using vector data for antialiasing image data, col. 2, lines 20-56. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in the bit map representation disclosed in Nishida the vector representation for character and graphics data as disclosed in Kumazaki, because in antialiasing vector image processing techniques produce smoother edge portions of output images than in a bit map.

With respect to dependent claim 31, . . . determining luminance comprises counting a number of bits on in the portion of the bit map corresponding to a pixel. Nishida discloses a number of bits larger than the divisional level of the display for displaying the shape to be displayed, col. 11, lines16-67. Nishida discloses display signals corresponding to the resolutions of display devices to select commands to display the picture at a corresponding resolution of the divisional level, col. 22, lines 49-67.

With respect to dependent claims 32 and 33, the size larger . . . is at least (ten times) twice as wide as the particular size.

Nishida discloses display signals corresponding to the resolutions of display devices to select commands to display the picture at a corresponding resolution of the divisional level, col. 22, lines 49-67.

With respect to dependent claim 34, . . . the shape comprises a character. Nishida discloses in figure 21A.

With respect to dependent claims 35-37, . . . the display comprising a (television; color television; display of hand held device; billboard.)

Nishida discloses display devices such as attached on a wall, col. 1, lines 4-7.

With respect to dependent claim 38, . . . logic for communication with the Internet.

However, it is noted that Nishida fails to disclose communication with the Internet and web browser logic.

Kumazaki discloses a receiving/transmitting in the input output unit, col. 10, lines 1-21.

It would have been obvious to one of ordinary skill in the art at the time of the invention of Nishida to include logic for communicating with the Internet and web browsers as disclosed in Kumazaki to provide display capabilities for every pixel element of characters or picture in an entire display area.

With respect to dependent claim 67, logic that renders the bit map is not particularly adapted to be used with the logic that determines luminances. Nishida discloses signals for the display devices having different resolution and storing commands to deliver commands from the control unit for divisional levels and displaying

different resolution of the divisional levels, col. 22, lines 49-67, separate from the instructions for determining luminance, col. 19, lines 1-21.

As per independent claim 68, a method of display a set of characters, the method comprising: in a system having a specific hardware device that has a specific resolution, receiving a command to generate the character; if the character has already been processed and is available in a cache, displaying the character, if the character has not already been processed, taking the resolution of the hardware display device into consideration . . .

Nishida discloses a number of bits larger than the divisional level of the display for displaying the shape to be displayed, col. 11, lines 16-67. Nishida discloses display signals corresponding to the resolutions of display devices to select commands to display the picture at a corresponding resolution of the divisional level, col. 22, lines 49-67.

However, it is noted that Nishida fails to disclose a cache for storing characters already processed. Nishida discloses memory, figure 9. It would have been obvious to one of ordinary skill in the art at the time of the invention to include storing processed characters to deliver high-speed operations.

(11) Response to Argument

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the applicant argues that Nishida.

Applicant agues that Nishida fails to disclose receiving a command to generate the shape displayed a particular size on a display and furthermore requesting a bit map rendering of the shape larger than the particular size. Nishida disclose changing a display state of a pixel in a display device, a control unit, which delivers a display signal for designating display states including divisional level information, col. 2, lines 30-67. Nishida discloses in figures 21A-21D, views showing display states having different resolutions, and further discloses carrying out a proper display process based on the resolution of the display device even if various display signals with various resolutions are delivered, col. 19, lines 22-29 and further discloses picture processing such as enlargement, shrinkage, movement or rotation can be easily implemented as occasion demands, col. 20, lines 53-64. Therefore it is the position of the Examiner that Nishida allows for receiving demands for the shape to be enlarged, or larger than a particular size.

Applicant argues that Nishida fails to disclose a system with a display having a particular number of bits greater than the divisional level and requesting a bit map rendering of a shape larger than the particular size to be displayed. Nishida further discloses in enlargement of an image shifting the address in any direction by 2 bits, col.

20, lines 53-67, therefore providing the corresponding bit map rendering of the shape larges than the size in which the shape is to be displayed. Furthermore, it is well known in the art that for an image to be displayed on a display device, the display attributes are necessary for accurate display of the image.

Applicant argues that in independent claim 68, Nishida fails to disclose if the character has been processed and available in a cache displaying the character. Examiner referred in the office action to Nishida as disclosing memory, and cache is a form of storage.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., antialiasing) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that Examiner fails to provide teaching or suggestion for delivering high-speed operations. Examiner's secondary reference, Kumazaki discloses improved antialiasing process carried out at a high speed to reduce the effects of aliasing for edge portions, col. 1, lines 8-15, and further discloses storing in a prescribed LUT the pixels of the portion of the image, col. 7, lines 15-21, and utilizing vector representation.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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February 5, 2004

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